# SEMICONDUCTOR DEVICE WITH FLEXIBLE REDUNDANCY SYSTEM

## CROSS-REFERENCE TO RELATED APPLICATIONS

[01] This application is a continuation of prior application serial no. 10/348,965, filed January 23, 2003, now Patent No. 6,717,871 which is a continuation of prior application serial no. 10/310,960, filed December 6, 2002, which is a continuation of prior application serial no. 09/953,307, filed September 17, 2001, now Patent No. 6,542,420 which is a continuation of prior application serial no. 09/739,240, now Patent No. 6,314,032 filed December 19, 2000, now U.S. patent no. 6,314,032, which is a continuation of prior application serial no. 09/296,269, filed April 22, 1999, now U.S. patent no. 6,188,618, which claims priority under 35 U.S.C. § 119 to Japanese patent application 11-108096, filed April 15, 1999 and Japanese patent application 10-112967, filed April 23, 1998. The entire disclosures of the prior applications are hereby incorporated by reference herein.

## BACKGROUND OF THE INVENTION

[02] This invention relates to a semiconductor device with a flexible redundancy system for saving a defective memory cell.

[03] Semiconductor devices have a redundancy system. To enhance the yield of products, the redundancy system saves a defective memory cell, if any, by replacing it with a redundancy cell. The redundancy system that is most generally used at the present stage performs such replacement in units of a cell array, more specifically in units of a plurality of rows or columns (there is a case where it is done in units of one row or column). If in this system, a defective memory cell is found after a test, a cell array including the defective cell is replaced with a redundancy cell array (spare element) of the same size.

[04] Address information on a cell array including the defective cell is stored in a non-volatile storage element. A fuse is generally used as the storage element at the present stage. Since the address information is usually formed of several bits, a fuse set which